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09/326,785	06/04/1999	ERICH FRANZ HARATSCH	1-4	4629

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EXAMINER	
KUMAR, PANKAJ	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/326,785	Applicant(s) HARATSCH ET AL.
	Examiner Pankaj Kumar	Art Unit 2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5,7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. DETAILED ACTION

2. Specification

3. The abstract of the disclosure is objected to because it is too long. Abstract needs to be between 50 and 150 words. Correction is required. See MPEP § 608.01(b).

4. Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

6. A person shall be entitled to a patent unless –

7. (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 1, 4, 6, 7, 10, 13, 19-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Endres et al. USPN 6426972B1.

10. As per claim 1, Endres teaches a method for processing a signal received from a dispersive channel (Endres fig. 1: since the system requires matched filtering 114 and equalizer

120, the channel is dispersive), said channel having a memory length, L, and being modeled as a filter having L taps (inherent for filters to have taps and each tap requires one delay element and thus the delay element is the memory), said method comprising the steps of:

11. processing less significant taps with a lower complexity cancellation algorithm that cancels the less significant taps using tentative decisions (Endres fig. 4: 414, 416, 420, "zero p0 taps"; tentative decision are in 416 and 420 since they make tentative decisions); and processing more significant taps with a reduced state sequence estimation (RSSE) technique (Endres Abstract: "The slicer identifies an encoded VSB symbol by partial trellis decoding and quantization from a reduced-set constellation."; fig. 13 indicates path length of 1 or 2 while fig. 14 has a path length of 2 and thus fig 13 provides for reduced state (path length reduced from 2 to possibly 1) sequence estimation).

12. As per claim 4, Endres teaches the method according to claim 1, wherein said lower complexity cancellation algorithm reduces the intersymbol interference (Endres col. 2 lines 1-2 "ghost cancellation") associated with said less significant taps (Endres in fig. 4 just zeros the taps which in claim 1 were defined to be the less significant taps; by zeroing the taps, ISI is also reduced).

13. As per claim 6, Endres teaches the method according to claim 1, further comprising the step of sampling said signal (Endres fig. 1 inherent to sample when receiving signals).

Claim 19 has been cancelled.

Claim 20 has been cancelled.

Claim 21 has been cancelled.

Claim 23 has been added as:

Claim ~~23~~ 6---The method according to claim 1, wherein a partial decision feedback equalization filtering technique processes said intersymbol interference due to said less significant taps.---

Claim 24 has been added as:

Claim ~~24~~ 7.---The method according to claim 1, wherein said reduced state sequence estimation technique estimates intersymbol interference terms based on a path history of each state.---

Claim 25 has been added as:

Claim ~~25~~ 8.---The method according to claim 5, wherein said intersymbol interference due to said U more significant taps is processed with said reduced state sequence estimation technique for each state based on survivor symbols.---

Claim 26 has been added as:

Claim ~~26~~ 19.---The receiver according to claim ~~10~~ 11, wherein said reduced state sequence estimation technique has a survivor memory unit with a survivor memory depth D that is smaller than L.---

Claim 27 has been added as:

Claim ~~27~~ 16.--The receiver according to claim ~~14~~ 15, wherein a filter section with L-U filter taps that uses said tentative decisions processes said intersymbol interference due to said less significant taps.---

Remarks:

14. As per claim 7, Endres teaches the method according to claim 1, further comprising the step of digitizing said signal (Endres col. 3 lines 55-56 "The RF demodulator 110 also generates digital samples of the RF signal.").

15. As per claim 10, Endres teaches a receiver that receives a signal from a dispersive channel (Endres fig. 1: since the system requires matched filtering 114 and equalizer 120, the channel is dispersive), said channel having a memory length, L, and being modeled as a filter having L taps (inherent for filters to have taps and each tap requires one delay element and thus the delay element is the memory), comprising: a tentative decision/tail processing circuit for processing less significant taps with a lower complexity cancellation algorithm (Endres fig. 4: 414, 416, 420, "zero p0 taps" ; tentative decision are in 416 and 420 since they make tentative decisions); and a reduced state sequence estimation (RSSE) circuit for processing only the more significant taps (Endres Abstract: "The slicer identifies an encoded VSB symbol by partial trellis decoding and quantization from a reduced-set constellation."; fig. 13 indicates path length of 1 or 2 while fig. 14 has a path length of 2 and thus fig 13 provides for reduced state (path length reduced from 2 to possibly 1) sequence estimation; it is only the more significant taps since fig. 4 shows 424 cancels the less significant taps by zeroing the taps and 422 fixes the P1 taps, which are the more significant taps, to be used in filtering).

16. Claim 13 is discussed in regards to clam 4.

17. As per claim 19, Endres teaches a method for processing a signal received from a dispersive channel (Endres fig. 1: since the system requires matched filtering 114 and equalizer 120, the channel is dispersive), said channel having a memory length, L, and being modeled as a filter having L taps (inherent for filters to have taps and each tap requires one delay element and thus the delay element is the memory), said method comprising the steps of processing less significant taps with a first algorithm of first complexity (Endres fig. 4: 414, 416, 420, "zero p0 taps" ; tentative decision are in 416 and 420 since they make tentative decisions); and processing more significant taps with a second algorithm of second complexity that is greater than said first complexity (Endres Abstract: "The slicer identifies an encoded VSB symbol by partial trellis decoding and quantization from a reduced-set constellation."; fig. 13 indicates path length of 1 or 2 while fig. 14 has a path length of 2 and thus fig 13 provides for reduced state (path length reduced from 2 to possibly 1) sequence estimation; it is only the more significant taps since fig. 4 shows 424 cancels the less significant taps by zeroing the taps and 422 fixes the P1 taps, which are the more significant taps, to be used in filtering).

18. Claims 20 and 21 are discussed in regards to claim 19.

19. As per claim 22, Endres teaches a receiver that receives a signal from a dispersive channel (Endres fig. 1: since the system requires matched filtering 114 and equalizer 120, the channel is dispersive), said channel having a memory length, L, and being modeled as a filter having L taps (inherent for filters to have taps and each tap requires one delay element and thus the delay element is the memory), comprising: means for processing less significant taps with a

lower complexity cancellation algorithm that cancels the less significant taps using tentative decisions (Endres fig. 4: 414, 416, 420, "zero p0 taps"; tentative decision are in 416 and 420 since they make tentative decisions); and means for processing more significant taps with a reduced state sequence estimation (RSSE) technique (Endres Abstract: "The slicer identifies an encoded VSB symbol by partial trellis decoding and quantization from a reduced-set constellation."; fig. 13 indicates path length of 1 or 2 while fig. 14 has a path length of 2 and thus fig 13 provides for reduced state (path length reduced from 2 to possibly 1) sequence estimation; it is only the more significant taps since fig. 4 shows 424 cancels the less significant taps by zeroing the taps and 422 fixes the P1 taps, which are the more significant taps, to be used in filtering).

20. Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

22. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 2, 3, 5, 11, 12, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endres.

24. As per claim 2, Endres teaches the method according to claim 1 with a decision-feedback equalizer (DFE) technique (Endres: "The exemplary adaptive equalizer structure is shown in FIG. 2A. This equalizer includes a forward or finite impulse response (FIR) section 216 and a

feedback or infinite impulse response (IIR) section 230."; since it is adaptive, decisions need to be made). What Endres does not show is wherein said lower complexity cancellation algorithm is a decision-feedback equalizer (DFE) technique. Instead Endres is showing a higher complexity cancellation algorithm is a decision-feedback equalizer (DFE) technique. It would have been obvious to one skilled in the art at the time of the invention to modify Endres to show DFE as a lower complexity cancellation algorithm since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

25. As per claim 3, Endres teaches the method according to claim 1 with a soft decision-feedback equalizer (DFE) technique (Endres figs. 13, 14 indicate soft decision inputs into 930 from fig. 9.). What Endres does not teach is wherein said lower complexity cancellation algorithm is a soft decision-feedback equalizer (DFE) technique. Instead what Endres teaches is wherein said higher complexity cancellation algorithm is a soft decision-feedback equalizer (DFE) technique. It would have been obvious to one skilled in the art at the time of the invention to modify Endres to show soft DFE as a lower complexity cancellation algorithm since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

26. As per claim 5, Endres teaches the method according to claim 1. What Endres does not teach is wherein said more significant taps comprise taps below a tap number, U, where U is a prescribed number less than L. What Endres does teach is wherein said more significant taps (Endres fig. 4: P1 taps) comprise taps ABOVE a tap number, U (Endres fig. 4: delta), where U is

a prescribed number less than L (can assume L to be infinity). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make more significant taps, taps above a certain number rather than taps below a certain number, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art. In re Einstein, 8 USPQ 167.

27. Claim 11 is discussed in regards to claim 2.

28. Claim 12 is discussed in regards to claim 3.

29. Claim 14 is discussed in regards to claim 5.

30. Claims 8, 9, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endres in view of Wei USPN 6151370.

31. As per claim 8, Endres teaches the method according to claim 1. What Endres does not teach is wherein said reduced state sequence estimation (RSSE) technique is a decision-feedback sequence estimation (DFSE) technique. What Wei teaches is wherein said reduced state sequence estimation (RSSE) technique (Wei "The invention may also be contrasted with prior art where, in order to reduce decoder complexity, a reduced-state state-oriented Viterbi decoder is used in which the surviving paths leading into only a reduced number of states are retained.") is a decision-feedback sequence estimation (DFSE) technique (Wei fig. 6: 620). It would have been

obvious to one skilled in the art at the time of the invention to modify Endres with the DFSE in Wei. One would be motivated to do so to reduce ISI as indicated in Wei.

32. As per claim 9, Endres teaches the method according to claim 1. What Endres does not teach is wherein said reduced state sequence estimation (RSSE) technique is a parallel decision-feedback equalization (PDFE) technique. What Wei teaches is wherein said reduced state sequence estimation (RSSE) technique (Wei "The invention may also be contrasted with prior art where, in order to reduce decoder complexity, a reduced-state state-oriented Viterbi decoder is used in which the surviving paths leading into only a reduced number of states are retained.") is a parallel decision-feedback equalization (PDFE) technique (Wei fig. 6: 620 shows DFEs in parallel). It would have been obvious to one skilled in the art at the time of the invention to modify Endres with the PDFE in Wei. One would be motivated to do so for a more efficient system.

33. Claim 15 is discussed in regards to claim 8.

34. Claim 16 is discussed in regards to claim 9.

35. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endres in view of Molnar et al. USPN 6081566.

36. As per claim 17, Endres teaches a method for processing a signal received from a dispersive channel (Endres fig. 1: since the system requires matched filtering 114 and equalizer 120, the channel is dispersive), said channel having a memory length, L, and being modeled as a filter having L taps (inherent for filters to have taps and each tap requires one delay element and thus the delay element is the memory), said method comprising the steps of processing less significant taps with a lower complexity cancellation algorithm that cancels the less significant taps using tentative decisions (Endres fig. 4: 414, 416, 420, "zero p0 taps" ; tentative decision are in 416 and 420 since they make tentative decisions). What Endres does not teach is processing more significant taps with an M-algorithm (MA) technique. What Molnar teaches is using the M-algorithm (MA) technique (Molnar col. 7 line 54) for filtering (Molnar col. 7 first full paragraph) which is equivalent to processing taps. It would have been obvious to one skilled in the art at the time of the invention to modify Endres RSSE with Molnar's M-algorithm (MA) technique. One would be motivated to do so since Molnar teaches, "As will be apparent to one skilled in the art, other sequence estimation algorithms, such as the M-algorithm, may also be used."

37. As per claim 18, Endres teaches a receiver that receives a signal from a dispersive channel (Endres fig. 1: since the system requires matched filtering 114 and equalizer 120, the channel is dispersive), said channel having a memory length, L, and being modeled as a filter having L taps (inherent for filters to have taps and each tap requires one delay element and thus the delay element is the memory), comprising: a tentative decision/tail processing circuit for processing less significant taps with a lower complexity cancellation algorithm (Endres fig. 4:

414, 416, 420, "zero p0 taps" ; tentative decision are in 416 and 420 since they make tentative decisions). What Endres does not teach is a sequence estimation circuit that implements an M-algorithm (MA) for processing only the more significant taps. What Molnar teaches is a sequence estimation circuit that implements an M-algorithm (MA) (Molnar col. 7 line 54) for filtering (Molnar col. 7 first full paragraph) which is equivalent to processing taps. It would have been obvious to one skilled in the art at the time of the invention to modify Endres RSSE with Molnar's M-algorithm (MA) technique. One would be motivated to do so since Molnar teaches, "As will be apparent to one skilled in the art, other sequence estimation algorithms, such as the M-algorithm, may also be used."

38. Conclusion

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Agazzi et al. USPN 6201831B1; IEEE "Reduced State Sequence Estimation for Coded Modulation on Intersymbol Interference Channels" page 2 2nd column states "RSSE reduces to ... PDFD"

40. As per claim 1, Agazzi teaches a method for processing a signal received from a dispersive (Agazzi fig. 2: 232 is an echo canceller which means the channel has an echo component and thus the channel is dispersive) channel (Agazzi fig. 2: 232, 230, 228, 212), said channel having a memory length, L, and being modeled as a filter having L taps (inherent for filters to have taps and each tap requires one delay element and thus the delay element is the memory), said method comprising the steps of: processing less significant taps with a lower complexity cancellation algorithm that cancels the less significant taps using tentative decisions

(Agazzi fig. 2: processing lower frequencies with 234 and 232, 230, 228); and processing more significant taps (Agazzi fig, 2 processing high frequencies with 212) with a reduced state sequence estimation (RSSE) technique.

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

42. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

43. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

44. 45.

46. PK
47. August 8, 2002

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 8/12/02